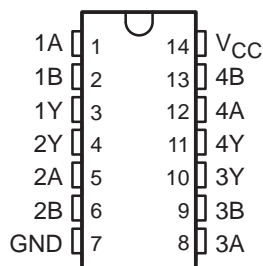


SN54HC266, SN74HC266 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-DRAIN OUTPUTS

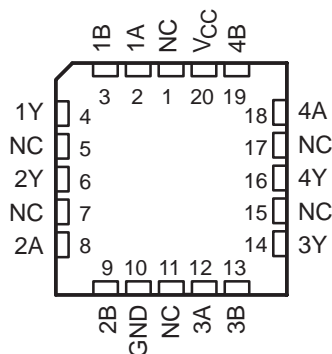
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- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Inverting Outputs Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 10$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

SN54HC266 . . . J OR W PACKAGE
SN74HC266 . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54HC266 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC266 devices have four independent 2-input exclusive-NOR gates and feature open-drain outputs. They perform the Boolean function $Y = A \otimes B$ or $Y = AB + AB$ in positive logic.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|--------------|-----------------------|------------------|
| –40°C to 85°C | PDIP – N | Tube of 25 | SN74HC266N | SN74HC266N |
| | SOIC – D | Tube of 50 | SN74HC266D | HC266 |
| | | Reel of 2500 | SN74HC266DR | |
| | | Reel of 250 | SN74HC266DT | |
| –55°C to 125°C | SOP – NS | Reel of 2000 | SN74HC266NSR | HC266 |
| | CDIP – J | Tube of 25 | SNJ54HC266J | SNJ54HC266J |
| | CFP – W | Tube of 150 | SNJ54HC266W | SNJ54HC266W |
| | LCCC – FK | Tube of 55 | SNJ54HC266FK | SNJ54HC266FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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SN54HC266, SN74HC266

QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES

WITH OPEN-DRAIN OUTPUTS

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FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | H |

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|---------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |

Storage temperature range, T_{stg} –65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | | SN54HC266 | | | SN74HC266 | | | UNIT |
|-----------------|---------------------------------|-------------------------|-----------|-----------------|-----|-----------|-----------------|-----|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | | | 1.5 | | | V |
| | | V _{CC} = 4.5 V | 3.15 | | | 3.15 | | | |
| | | V _{CC} = 6 V | 4.2 | | | 4.2 | | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | | | 0.5 | | | V |
| | | V _{CC} = 4.5 V | | | | 1.35 | | | |
| | | V _{CC} = 6 V | | | | 1.8 | | | |
| V _I | Input voltage | | 0 | V _{CC} | | 0 | V _{CC} | | V |
| V _O | Output voltage | | 0 | V _{CC} | | 0 | V _{CC} | | V |
| Δt/Δv | Input transition rise/fall time | V _{CC} = 2 V | 1000 | | | 1000 | | | ns |
| | | V _{CC} = 4.5 V | 500 | | | 500 | | | |
| | | V _{CC} = 6 V | 400 | | | 400 | | | |
| T _A | Operating free-air temperature | | −55 | 125 | | −40 | 85 | | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54HC266, SN74HC266
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES
WITH OPEN-DRAIN OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54HC266 | | SN74HC266 | | UNIT |
|-----------------|--|--------------------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| I _{OH} | V _I = V _{IH} or V _{IL} , V _O = V _{CC} | 6 V | | 0.01 | 0.5 | | 10 | | 5 | μA |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | I _{OL} = 4 mA | 4.5 V | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | I _{OL} = 5.2 mA | 6 V | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| I _I | V _I = V _{CC} or 0 | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | 6 V | | | 2 | | 40 | | 20 | μA |
| C _i | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN54HC266 | | SN74HC266 | | UNIT |
|------------------|--------------|-------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | Y | 2 V | | 60 | 125 | | 190 | | 155 | ns |
| | | | 4.5 V | | 13 | 25 | | 38 | | 31 | |
| | | | 6 V | | 10 | 23 | | 32 | | 26 | |
| t _{PHL} | A or B | Y | 2 V | | 60 | 100 | | 150 | | 125 | ns |
| | | | 4.5 V | | 13 | 20 | | 30 | | 25 | |
| | | | 6 V | | 10 | 17 | | 25 | | 21 | |
| t _t | | Y | 2 V | | 28 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

operating characteristics, T_A = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------------|--|-----------------|-----|------|
| C _{pd} | Power dissipation capacitance per gate | No load | 35 | pF |

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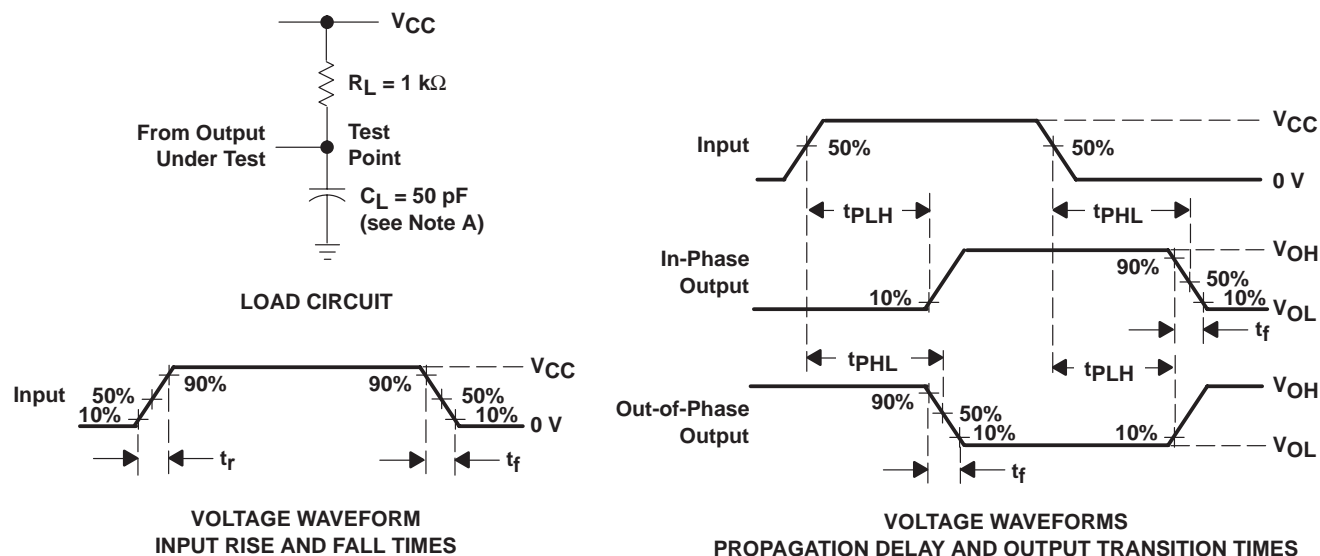
SN54HC266, SN74HC266

QUADRUPL 2-INPUT EXCLUSIVE-NOR GATES

WITH OPEN-DRAIN OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$.
 - C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74HC266D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266DT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266DTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266DTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74HC266NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74HC266NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266NSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC266NSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

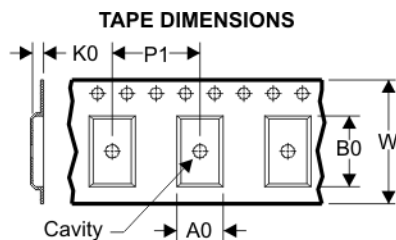
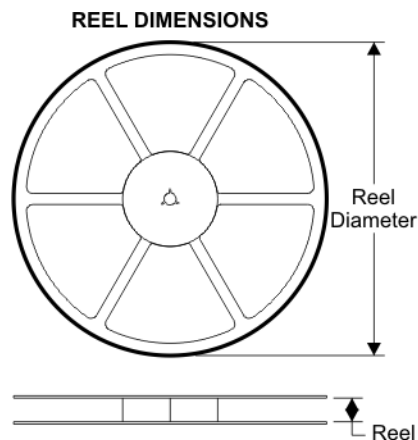
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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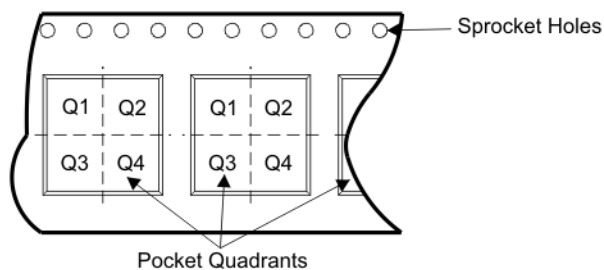
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TAPE AND REEL BOX INFORMATION



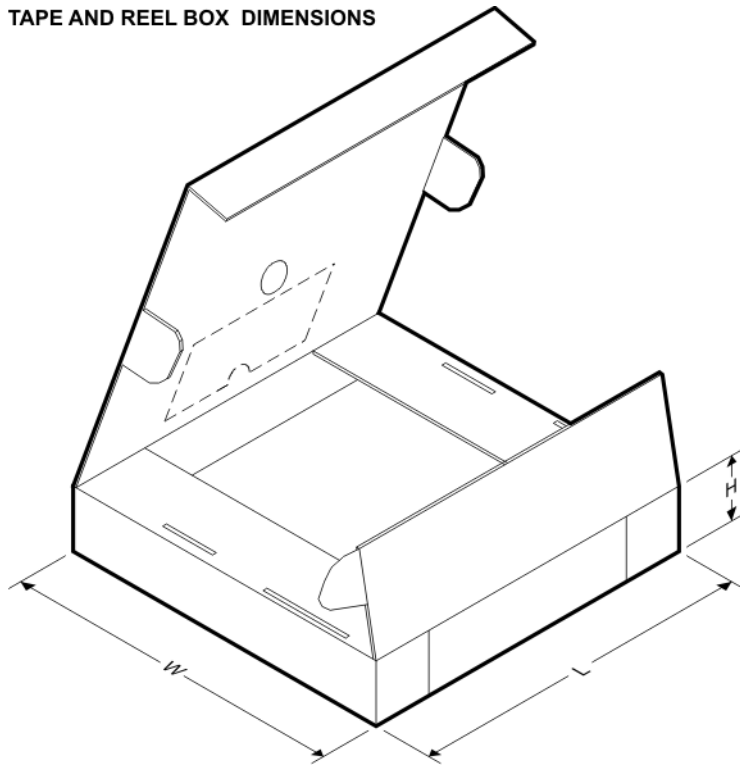
| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|---------|------|---------|--------------------|-----------------|---------|---------|---------|---------|--------|---------------|
| SN74HC266DR | D | 14 | SITE 41 | 330 | 16 | 6.5 | 9.0 | 2.1 | 8 | 16 | Q1 |
| SN74HC266NSR | NS | 14 | SITE 41 | 330 | 16 | 8.2 | 10.5 | 2.5 | 12 | 16 | Q1 |

TAPE AND REEL BOX DIMENSIONS

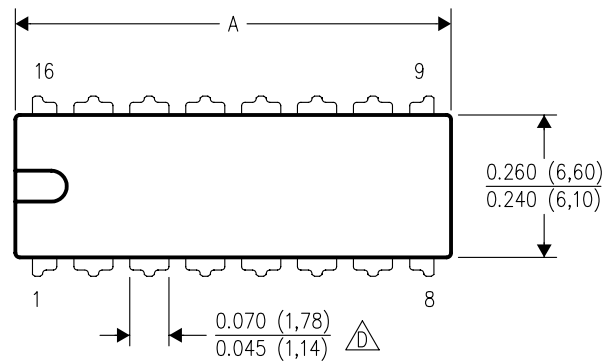


| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|--------------|---------|------|---------|-------------|------------|-------------|
| SN74HC266DR | D | 14 | SITE 41 | 346.0 | 346.0 | 33.0 |
| SN74HC266NSR | NS | 14 | SITE 41 | 346.0 | 346.0 | 33.0 |

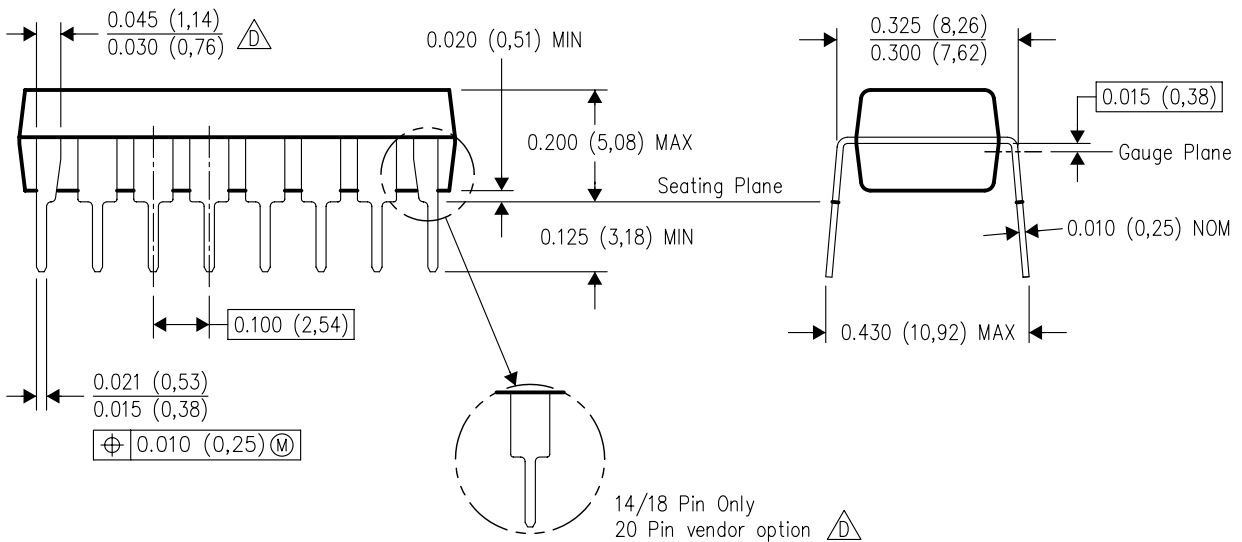
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |

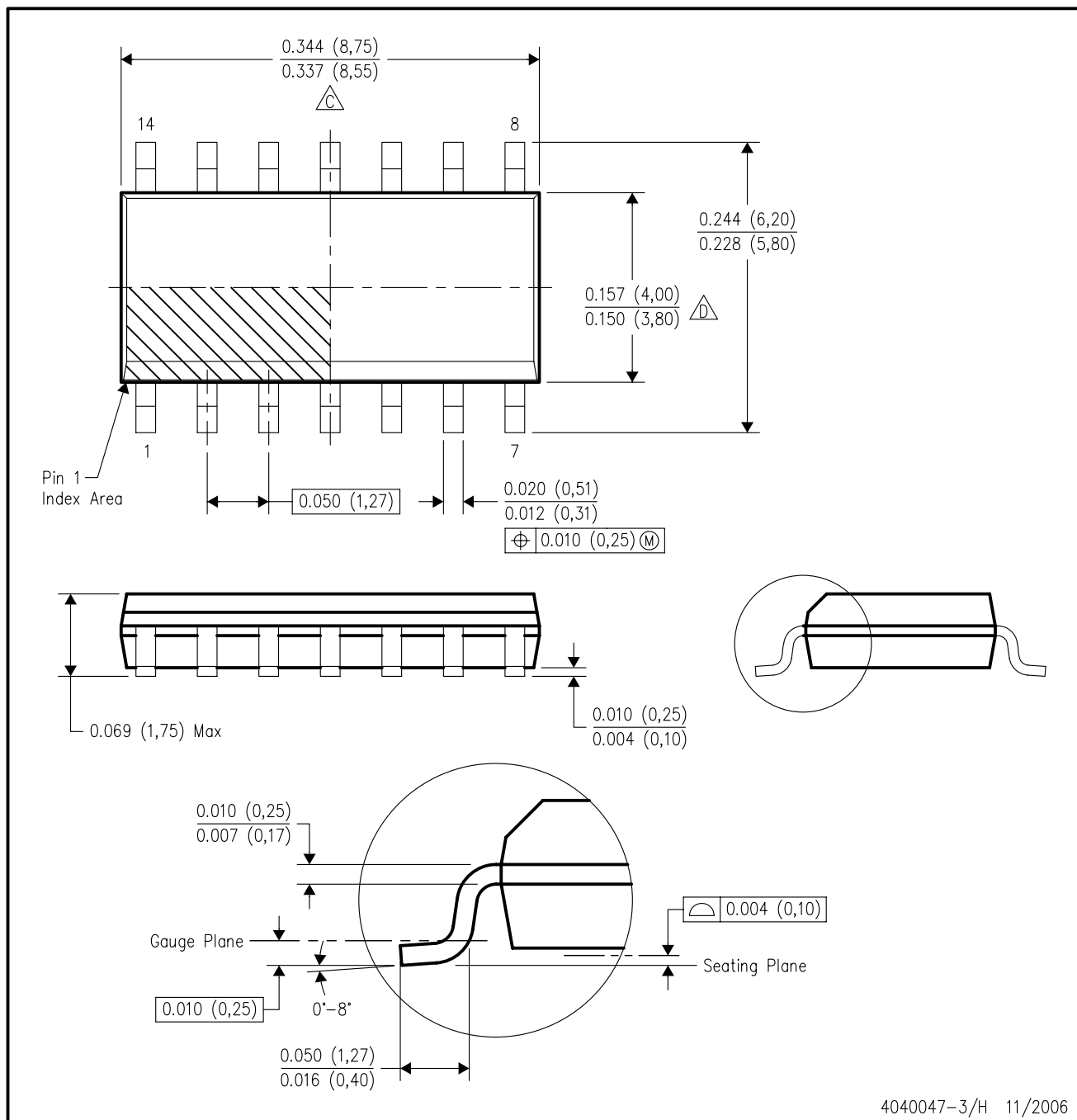


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/H 11/2006

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---------------|-------|-------|-------|-------|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.